

PROGRAMME
of the Joint 6th SemOI Workshop & 1st Ukrainian-French SOI Seminar

1st day (Monday, April 26)

a.m.

9⁰⁰ Opening ceremony

Ukrainian-French Seminar

9³⁰ **(Invited) Silicon-based devices and materials for nanoscale FETs**

F. Balestra

MINATEC, SINANO, France

10⁰⁰ **(Invited) Selected SOI puzzles and tentative answers**

K-I. Na,¹ W. Van Den Daele,¹ L. Pham-Nguyen,¹ M. Bawedin,¹ K-H. Park,¹ J. Wan,¹ K. Tachi,^{1,2} S-J. Chang,¹ I. Ionica,¹ Y-H. Bae,^{1,3} J.A. Chroboczek,¹ C. Fenouillet-Beranger,^{2,4} T. Ernst,² E. Augendre,² C. Le Royer,² A. Zaslavsky,^{1,5} H. Iwai,⁶ **S. Cristoloveanu**¹

¹*IMEP-LAHC, Grenoble INP Minatec, France*

²*CEA-LETI, Minatec, France*

³*Uiduk University, Gangdong, Gyeongju, Korea*

⁴*STMicroelectronics, Crolles Cedex, France*

⁵*Division of Engineering, Brown University, Providence, USA*

⁶*Frontier Research Center, Tokyo Institute of Technology, Yokohama, Japan*

10³⁰ **(Invited) From ultra thin silicon SOI to FDSOI devices**

C. Mazuré, Bich-Yen Nguyen, Walter Schwarzenbach, Daniel Delpra, Konstantin Bourdelle
SOITEC, Bernin, France

11⁰⁰ **Coffee break**

Ukrainian-French Seminar

11³⁰ **(Invited) Ultrathin body SOI transistors for 22 nm technology node and beyond**

T. Poiroux, F. Andrieu, O. Weber, C. Fenouillet-Béranger, C. Buj-Dufournet, P. Perreau, L. Tosti, L. Brevard and O. Faynot

CEA-LETI, MINATEC, France

12⁰⁰ **(Invited) Special Features of the Back-Gate Effects in UTB SOI MOSFETs**

T.E. Rudenko¹, V. Kilchytska², J.-P. Raskin², F. Andrieu³, O. Faynot³, Y. Le Tiec³, K. Landry⁴, A. Nazarov¹, and D. Flandre²

¹*Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine*

²*Université catholique de Louvain, Louvain-la-Neuve, Belgium*

³*CEA-LETI MINATEC, Grenoble, France*

⁴*SOITEC, Bernin, France*

12³⁰ **(Invited) Amorphous silicon-carbon alloy films on SOI as a functional material for MEMS technologies**

A.V. Vasin¹, A.V. Rusavsky¹, V.S. Lysenko¹, A.N. Nazarov¹, Yu. Ishikawa², Sh. Muto³, T. Kimura³, N. André⁴ and J.-P. Raskin⁴

¹*Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine*

²*Japan Fine Ceramics Center, Nagoya, Japan*

³*Department of Materials, Physics and Energy Engineering, Nagoya University, Japan*

⁴*Université catholique de Louvain, Louvain-la-Neuve, Belgium*

13⁰⁰ **Lunch**

p.m.

SemOI WORKSHOP

SOI Material and Devices Technologies

14³⁰ **(Invited) High Resistivity SOI wafer: the substrate for RF SoC applications?**

J.-P. Raskin

Université catholique de Louvain, Microwave Laboratory, Louvain-la-Neuve, Belgium

15⁰⁰ **(Invited) GeOI Technology**
H.S. Gamble, P.T. Baine, Y.W. Low, Y.H. Low, P.V. Rainey, R. Hurley, J.H. Montgomery, B.M. Armstrong, D.W. McNeill, S.J.N. Mitchell
School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, N. Ireland

15³⁰ **(Invited) ZnO films and nanocrystals on bulk silicon and SOI wafers: formation, properties and applications**
E. Chubenko¹, M. Balucani², A. Belous³, V. Malyshev³, **V. Bondarenko**¹
¹*Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus*
²*University of Rome "La Sapienza", Rome, Italy*
³*Research and Development Centre "Belmicrosystems", Integral Corporation, Minsk, Belarus*

16⁰⁰ **Coffee break**

SOI Material and Devices Technologies

16³⁰ **(Invited) Low temperature fabrication of germanium-on-insulator (GeOI) structure using remote plasma activation and hydrogen exfoliation**
C. Colinge¹, K.Y. Byun¹, I. Ferain¹, M. Goorsky²
¹*Tyndall National Institute, University College Cork, Cork, Ireland*
²*Department of Material Science and Engineering, UCLA, USA*

17⁰⁰ **The investigation on the interface characteristics of GeOI manufactured by low temperature wafer bonding**
X. X. Zhang^{1,2}, T.C. Ye¹, S. Zhuang², J. Jiao³
¹*Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China*
²*Shanghai Key Laboratory of Modern Optical System University of Shanghai for Science and Technology Shanghai, China*
³*Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences Shanghai, China*

17²⁰ **(Invited) Fabrication and characterization of strained semiconductor materials on dielectric platforms**
D. Leadley
University of Warwick, UK

17⁵⁰ **SOI structures with nitrided buried SiO₂ layer: formation and properties**
I.E. Tyschenko, V.P. Popov
Institute of Semiconductor Physics, Novosibirsk, Russia

2nd day (Tuesday, April 27)

a.m.

Ukrainian-French Seminar

9⁰⁰ **(Invited) Ohmic and Schottky contact CNTFET: transport properties and device performance using semi-classical and quantum particle simulation**
Ph. Dollfus, H.-N. Nguyen, D. Querlioz, A. Bournel and S. Retailleau
Institut d'Electronique Fondamentale, CNRS, Université Paris-Sud, Orsay, France

9³⁰ **(Invited) Confined and guided VLS growth of silicon nanoribbons: from nanowires to SOI-like layers**
A. Lecestre, **E. Dubois**, A. Villaret, T. Skotnicki, P. Coronel, G. Patriarche, C. Maurice
IEMN – UMR CNRS, Villeneuve d'Ascq, France

10⁰⁰ **(Invited) Gold assisted growth of silicon nanowires**
A.I. Klimovskaya, P.M. Lytvyn, Yu.N. Pedchenko, A.T. Voroschenko, O.C. Oberemok, A.V. Sarikov, O.A. Stadnik, Yu.M. Litvin, I.V. Prokopenko
Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine

10³⁰ **Coffee break**

Ukrainian-French Seminar

- 11⁰⁰ **(Invited) Engineering pseudosubstrates with porous silicon technology**
A. Boucherif, N. Blanchard, Ph. Regreny, A. Danescu, H. Magoarie, O. Marty, J. Penuelas, J.-M. Bluet, G. Guillot, V. Lysenko, and **G. Grenet**
Lyon Institute of Nanotechnologies, CNRS UMR, Université de Lyon, France
- 11³⁰ **(Invited) Photo-electrical properties of SiGe quantum dots on SiO_x**
Yu.N. Kozyrev¹, N.T. Kartel¹, M.Yu. Rubezhanska¹, S.V. Kondratenko², Ye.Ye. Melnichuk², C. Teichert³, V.S. Lysenko⁴, Yu.V. Gomeniuk⁴
¹*Institute of Surface Chemistry, NAS of Ukraine, Kyiv, Ukraine*
²*National Taras Shevchenko University, Kiev, Ukraine*
³*Institute of Physics, Montanuniversitaet Leoben, Leoben, Austria*
⁴*Institute of Semiconductor Physics, Kiev, Ukraine*
- 12⁰⁰ **(Invited) Multilayers porous silicon – silicon structures for sensors and solar cells**
V.A. Skryshevsky, I.I. Ivanov
Institute of High Technology, Taras Shevchenko National University, Kiev, Ukraine
- 12³⁰ **(Invited) 3D quantum simulation of elastic and inelastic scattering in Silicon nanowire FETs**
Marco Pala
IMEP-LAHC, INP Grenoble, Grenoble, France
- 13⁰⁰ **Lunch**

p.m.

SemOI WORKSHOP

Physics & Technology of New SOI devices

- 14³⁰ **(Invited) Junctionless transistors: physics and properties**
J.-P. Colinge, C.W. Lee, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti, R. Yu
Tyndall National Institute, University College Cork, Cork, Republic of Ireland
- 15⁰⁰ **(Invited) Floating body effects for SOI memories**
M. Bawedin¹, K-H. Park¹, K-I. Na¹, Y-H. Bae^{1,2} and S. Cristoloveanu¹
¹*IMEP-LAHC, Grenoble INP Minatec, France*
²*Uiduk University, Gangdong, Gyeongju, Korea*
- 15³⁰ **(Invited) FinFETs and their futures**
N. Horiguchi¹, B. Parvais¹, T. Chiarella¹, N. Collaert¹, A. Veloso¹, R. Rooyackers¹, P. Verheyen¹, L. Witters¹, A. Redolfi¹, A. De Keersgieter¹, S. Brus¹, G. Zschaetzsch^{1,2}, M. Erckena¹, E. Altamirano¹, S. Locorotondo¹, M. Demand¹, M. Jurczak¹, W. Vandervors^{1,2}, T. Hoffmann¹, and S. Biesemans¹
¹*IMEC, Leuven, Belgium*
²*Instituut voor Kern- en Stralingsfysica, K.U. Leuven, Leuven, Belgium*
- 16⁰⁰ **Towards SemOI-based quantum computers**
S. Filippov¹ and **V. Vyurkov**²
¹*Moscow Institute of Physics and Technology (State University), Russia*
²*Institute of Physics and Technology of the RAS, Moscow, Russia*
- 16²⁰ **Coffee break**

Physics&Theory of New SOI devices

- 16⁵⁰ **(Invited) Ultrathin single-gate and multiple-gate n-channel and p-channel SOI MOSFETs**
F. Gámiz, L. Donetti, C. Sampedro, A. Godoy, N. Rodriguez, F. Jimenez-Molinos
Nanoelectronics Research Group, Departamento de Electrónica, Universidad de Granada, Spain
- 17²⁰ **(Invited) Quantum simulation of an FD ETSOI FET**
A. Orlikovsky, V. Vyurkov, and I. Semenikhin
Institute of Physics and Technology of the Russian Academy of Sciences, Moscow, Russia
- 17⁵⁰ **(Invited) Some issues of modelling the double barrier metal-oxide-semiconductor tunnel structure**
B. Majkusiak and A. Mazurak

18²⁰ *Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland*
Break

19⁰⁰ **Poster Session & Buffet**

3rd day (Wednesday, April 28)

a.m.

Ukrainian-French Seminar

9⁰⁰ **(Invited) Single dopant and single electron effects in CMOS devices**

M. Sanquer

CEA-Grenoble, France

9³⁰ **(Invited) Mobility characterization in advanced FD-SOI CMOS devices**

G. Ghibaudo

IMEP-LAHC, MINATEC, Grenoble, France

10⁰⁰ **(Invited) Gate control of junction impact ionization avalanche in SOI MISFETs: theoretical model**

V. Dobrovolsky¹, **F. Sizov**¹, S. Cristoloveanu²

¹*Institute of Semiconductor Physics, Kiev, Ukraine*

²*IMEP, ENSERG, Grenoble, France*

10³⁰ **Coffee break**

SemOI WORKSHOP

Operation of Novel SOI devices

11⁰⁰ **(Invited) Influence of atomic fluctuation on operation nanoscaled devices**

S. Roy

Univ. of Glasgow, UK

11³⁰ **(Invited) Investigation of tri-gate FinFETs by noise methods**

N. Lukyanchikova¹, N. Garbar¹, V. Kudina¹, A. Smolanka¹, E. Simoen² and C. Claeys^{2,3}

¹*V. Lashkaryov Institute of Semiconductor Physics, Kiev, Ukraine*

²*IMEC, Leuven, Belgium*

³*Catholic University of Leuven, Leuven, Belgium*

12⁰⁰ **(Invited) SOI MOSFET transconductance behavior from micro to nano era**

J.A. Martino¹, P.G.D. Agopian¹, E. Simoen² and C. Claeys²

¹*LSI/PSI/USP - University of Sao Paulo, Brazil*

²*IMEC, Leuven, Belgium*

12³⁰ **Hydrogen gettering in processed oxygen-implanted silicon**

A. Misiuk¹, A. Barcz^{1,2}, A. Ulyashin³ and J. Bak-Misiuk²

¹*Institute of Electron Technology, Warsaw, Poland*

²*Institute of Physics, Warsaw, Poland*

³*SINTEF, Oslo, Norway*

13⁰⁰ **Lunch**

p.m.

14⁰⁰ **Excursion**

18⁰⁰ **Banquet**

4th day (Thursday, April 29)

a.m.

SemOI WORKSHOP

SOI Sensors and MEMS

9⁰⁰ **(Invited) Top-down processed SOI nanowire devices for biomedical applications**

S. Ingebrandt¹, X.T. Vu^{1,2}, J.F. Eschermann^{1,2}, R. Stockmann², A. Offenhäusse²

¹*Department of Informatics and Microsystem Technology, University of Applied Sciences Kaiserslautern, Germany*

²*Institute of Bio- and Nanosystems, Forschungszentrum Jülich, Germany*

9³⁰ **(Invited) Universal sensing platform of SOI nanowire transistor matrix for femtomole electronic bio and chemical sensors**

V.P. Popov¹, O.V. Naumova¹, Yu.D. Ivanov²

¹*Institute of Semiconductor Physics, Novosibirsk, Russia*

²*Institute of Biomedical Chemistry, Moscow, Russia*

10⁰⁰ **(Invited) Conceptual foundations of engineering and technology design for SOI microelectro-mechanical sensors with an integral monolithic tensoframe**

L.V. Sokolov

Federal State Unitary Enterprise Institute of Aircraft Equipment, Russia

10³⁰ **Non-standard FinFET devices for small volume sample sensors**

M. Zaborowski¹, **D. Tomaszewski**¹, L. Łukasiak², A. Jakubowski¹

¹*Institute of Electron Technology, Warsaw, Poland*

²*Warsaw University of Technology, Warsaw, Poland*

10⁵⁰ **Coffee break**

Novel SOI devices

11²⁰ **(Invited) Carbon: the future of silicon nanoelectronics?**

U. Schwalke

Institute for Semiconductor Technology and Nanoelectronics Technische Universität Darmstadt, Darmstadt, Germany

11⁵⁰ **(Invited) Variable barrier resonant tunneling transistor: performance investigation of a steep slope, high on-current device**

A. Afzalian¹, J.-P. Colinge² and D. Flandre¹

¹*Laboratoire de Microélectronique, Université Catholique de Louvain, Louvain-La-Neuve, Belgium*

²*Tyndall National Institute, University College Cork, Ireland*

12³⁰ **(Invited) Effects of high-energy neutrons on advanced SOI MOSFETs**

V. Kilchytska, J. Alvarado, O. Militaru, G. Berger, D. Flandre

Microelectronics Laboratory, Nuclear Physics Laboratory and Centre de Recherches du Cyclotron, Université catholique de Louvain, Louvain-la-Neuve, Belgium

13⁰⁰ **Lunch**

p.m.

14⁰⁰ **Excursion with visiting of Institutes of National Academy of Sciences**

Posters

- 1. Silicon-on-insulator flicker-noise gas sensor**
M.I. Makovychuk
Yaroslavl Branch of the Institute of Physics and Technology of RAS, Yaroslavl, Russia
- 2. Ion-beam synthesis of two-dimensional photonic crystals in silicon-on-insulator structures**
M.Yu. Barabanenkov¹, A.F. Vyatkin¹, A.I. Il'in¹, V.I. Zinenko¹, G.E. Daviduk², G.L. Myronchuk²
¹*Institute of Microelectronics Technology and superpure materials, Russian Academy of Sciences, Chernogolovka, Russia*
²*Lesya Ukrayinka Volyn' National University, Lutsk, Ukraine*
- 3. Influence hydrogen plasma treatment on a-SiC resistivity of the SiC/SiO₂/Si structures**
S. Gordienko¹, A. Nazarov¹, A. Rusavsky¹, A. Vasin¹, N. Rymarenko¹, V. Stepanov¹, T. Nazarova², V.P. Bondarenko³, K.I. Kholostov³, E.B. Chubenko³
¹*Lashkaryov Institute of Semiconductor Physics, NASU, Kyiv, Ukraine*
²*National Technical University of Ukraine "KPI", Kyiv, Ukraine*
³*Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus*
- 4. Semi-analytical models of field-effect transistors with low-dimensional channels**
A. Khomyakov and V. Vyurkov
Institute of Physics and Technology, Russian Academy of Sciences, Moscow, Russia
- 5. Research and development of technological processes of SOI for MEMS elements**
S.P. Timoshenkov¹, V.V. Kalugin¹, L.V. Sokolov², **N.M. Parfenov**²
¹*Moscow Institute of Electronics Engineering (Technical University), Moscow, Russia*
²*Moscow Aviation Institute (Technical University), Moscow, Russia* *Moscow Institute of Electronics*
- 6. Diamond – graphite heterostructures formed by nitrogen and hydrogen implantation and annealing**
V. P. Popov, L.N. Safronov, **O.V. Naumova**, Yu.N. Palyanov², I.N. Kupriyanov²
¹*Institute of Semiconductor Physics, Novosibirsk, Russia*
²*Institute of Geology and Mineralogy, Novosibirsk, Russia*
- 7. SOI heterostructures crystallographic features research**
K.L. Enisherlova, A.V. Lutzau, E.M. Temper, V.G. Gorjachev
Federal state unitary enterprise Science & Production enterprise "Pulsar", Moscow, Russia
- 8. Investigation electrical parameters of SOS-structures with 0,3 μ silicon layer**
K.L. Enisherlova¹, V.G. Gorjachev¹, E. L. Shobolov², V.A. Gerasimov²
¹*Federal state unitary enterprise "Science & Production enterprise Pulsar", Moscow, Russia*
²*Federal State Unitary Enterprise "Federal Research-and-Production Centre Measuring Systems Research Institute named after Yu.Ye.Sedakov", Nizhny Novgorod, Russian*
- 9. High temperature effect on harmonic distortions in submicron graded-channel MOSFETs**
M. Emam¹, M. A. Pavanello², F. Danneville³, D. Vanhoenacker-Janvier¹ and J.-P. Raskin¹
¹*Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium*
²*Department of Electrical Engineering, Centro Universitário da FEI, São Bernardo do Campo, Brazil.*
³*Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN), Villeneuve d'Ascq Cedex, France*
- 10. Model of nonuniform channel for the charge carrier transport in nanoscale FETs**
V. P. Popov, **M. A. Ilnitsky**
Institute of Semiconductor Physics, Novosibirsk, Russia
- 11. Double-gate voltage programmable silicon-nanowire-FETs**
F. Wessely, T. Krauss, U. Schwalke
Institute for Semiconductor Technology and Nanoelectronics, Darmstadt University of Technology, Darmstadt, Germany
- 12. Fabrication process for applying high mechanical stress on monocrystalline silicon film**
Vikram Passi¹, Umesh Bhaskar¹, Thomas Pardoen², Jean-Pierre Raskin¹

¹*Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium*

²*Institute of Mechanics, Materials and Civil Engineering, Université catholique de Louvain, Louvain-la-Neuve, Belgium*

13. Polysilicon on insulator structures for sensors application at harsh conditions

A.A.Druzhinin^{1,2}, I.T.Kogut³, Yu.M.Khoverko^{1,2}

¹*Lviv National Polytechnical University, SRC "Crystal"*

²*International Laboratory of High Magnetic Fields and Low Temperatures, Wroclaw, Poland*

³*Precarpathian university named after V. Stepanyk, Iv-Frankivsk Lviv National Polytechnical University, Lviv, Ukraine*

14. 3D SOI elements for silicon-on-chip applications

I. Kogut¹, A.A. Druzhinin², V. I. Golota¹

¹*Precarpathian National University, Ivano-Frankivsk, Ukraine*

²*National University "Lvivska Politechnika", Lviv, Ukraine*

15. A model of the evolution of the Au/Si droplet ensembles during rapid thermal annealing at high temperatures

A. Sarikov, A. Klimovskaya, O. Oberemok, O. Lytvyn, O. Stadnik

V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

16. SOI IC's for high-temperature operation

L.Samotovka

State Enterprise "Research Institute of Microdevices", Kiev, Ukraine

17. Electrical properties of high-k LaLuO₃ gate oxide for SOI MOSFETs

Y.Y. Gomeniuk¹, Y.V. Gomeniuk¹, A.N. Nazarov¹, P. Hurley², C. Cherkaoui², S. Monaghan², P.-E. Hellström³, O. Engström⁴

¹*V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine*

²*Tyndall NI, Cork, Ireland,*

³*KTH, Stockholm, Sweden*

⁴*Chalmers UT, Göteborg, Sweden*

18. Formation of Si nanocrystals in thin insulator SiO₂ by ion-plasma sputtering

A. Evtukh, V. Litovchenko, **O. Bratus**

V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

19. SIMOX technology with ultra-thin oxide layer and Si nanocluster inclusions

B. Romanjuk, V. Litovchenko, V. Melnik, V. Popov, O. Oberemok, V. Nikirin

V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

20. Charge trapping and retention in nanocrystal Non Volatile Memory structure

V.I. Turchanikov¹, V.A. Evtukh², **A.N. Nazarov**¹

¹*V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine*

²*Taras Shevchenko National University of Kyiv, Radio Physics Department, Kiev, Ukraine*